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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,083	08/06/2003	Richard W. Adkisson	200208999-2	7225
22879	7590	01/04/2008		
HEWLETT PACKARD COMPANY			EXAMINER	
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INTELLECTUAL PROPERTY ADMINISTRATION				
FORT COLLINS, CO 80527-2400			ART UNIT	PAPER NUMBER
			2863	
			NOTIFICATION DATE	DELIVERY MODE
			01/04/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/635,083	ADKISSON ET AL.
	Examiner Toan M. Le	Art Unit 2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 09 October 2007.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-36 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 06 August 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Ranson et al. (US Patent No. 5,887,003).

Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:  
an AND/OR circuit connected to receive the debug data (col. 12, lines 30-62);  
a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a current count value (col. 15, lines 56-67 to col. 16, lines 1-39); and

a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value (col. 12, lines 30-62; col. 11, lines 9-21; col. 15, lines 27-55; col. 19, lines 18-67; col. 20, lines 1-14),

wherein the AND/OR circuit activates the increment signal responsive to one or more selected bits of an events signal being set (col. 15, lines 56-67 to col. 16, lines 1-2; col. 16, lines 3-39).

As to claim 2, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the compare circuit comprises a match circuit for activating the match/threshold signal to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value (col. 15, lines 27-55).

Referring to claim 3, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the compare circuit comprises a threshold circuit for activating the match/threshold signal to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value (col. 12, lines 9-29).

As to claim 4, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising a select circuit connected to receive the debug data, the select circuit outputting to the compare circuit a selected block of the debug data identified by a value of a select control signal input thereto (col. 12, lines 30-62; col. 15, lines 27-55).

Referring to claim 5, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising a zero circuit connected to receive a portion of the selected debug data block from the select circuit, the zero circuit for zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto (col. 15, lines 56-67 to col. 16, lines 1-39).

As to claim 6, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the zeroed-out portion of the selected debug data block is input to the counter circuit and to the compare circuit (col. 15, lines 56-67 to col. 16, lines 1-39).

Referring to claim 7, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein, when the AND/OR circuit is operating in AND mode, the AND/OR circuit activates the increment signal when all of the selected bits of the events signal are set (col. 15, lines 27-55).

As to claim 8, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein when the AND/OR circuit is operating in OR mode, the AND/OR circuit activates the increment signal when at least one of the selected bits of the events signal is set (col. 15, lines 27-55).

Referring to claim 9, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected bits of the events signal are selected using a composite mask (col. 15, lines 27-55).

As to claim 10, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the events signal comprises the debug data, the match/threshold signal, and a logic one and wherein the composite mask signal comprises a debug data mask, a threshold/match mask, and an accumulate bit (col. 15, lines 27-55).

Referring to claim 11, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the debug data comprises 80 bits (Figures 8, 10).

As to claim 12, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks (Figures 8, 10).

Referring to claim 13, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected block comprises eight bits (Figures 8, 10).

As to claim 14, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the counter circuit comprises a 48-bit counter (Figure 13).

Referring to claim 15, Referring to claim 1, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein, when the counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value (col. 14, lines 64-67 to col. 15, lines 1-55; Figure 11).

As to claim 16, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the GPPC comprising:

an AND/OR circuit connected to receive the debug data (col. 12, lines 30-62);

a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated while the counter circuit is enabled, causes the counter circuit to increment a count value (col. 15, lines 56-67 to col. 16, lines 1-39); and

a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value (col. 12, lines 30-62; col. 11, lines 9-21; col. 15, lines 27-55; col. 19, lines 18-67; col. 20, lines 1-14),

wherein when the AND/OR circuit is in AND mode, the AND/OR circuit activates the increment signal if all of one or more selected bits of an events signal are set and when the AND/OR circuit is in OR mode, the AND/OR circuit activates the increment signal if at least one of the selected bits of the events signal is set (col. 15, lines 56-67 to col. 16, lines 1-2; col. 16, lines 3-39).

Referring to claim 17, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the compare circuit activates the match/threshold signal to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value and activates the match/threshold signal to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value (col. 12, lines 9-29).

As to claim 18, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising a select circuit connected to receive the debug data and output to the compare circuit a selected block of the debug data identified by a value of a select control signal input thereto (col. 12, lines 30-62; col. 15, lines 27-55).

Referring to claim 19, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising a zero circuit connected to receive a portion of the selected debug data block from the select circuit, the zero circuit for zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto and providing the zeroed-out portion of the selected debug data block to the counter circuit and to the compare circuit (col. 15, lines 56-67 to col. 16, lines 1-39).

As to claim 20, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the events signal comprises the debug data, the match/threshold signal, and a logic one (col. 15, lines 27-55).

Referring to claim 21, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected bits of the events signal are selected using a composite mask and wherein the composite mask signal comprises a debug data mask, threshold/match mask, and an accumulate bit (col. 15, lines 27-55).

As to claim 22, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the debug data comprises 80 bits (Figures 8, 10).

Referring to claim 23, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected block comprises 16 bits and the debug data comprises eight 10-bit-block-aligned blocks (Figures 8, 10).

As to claim 24, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the selected block comprises eight bits (Figures 8, 10).

Referring to claim 25, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein the count value is a 48-bit value (Figure 13).

As to claim 26, Ranson et al. disclose a general purpose performance counter ("GPPC") connected to a bus carrying debug data wherein, when the counter circuit is enabled, the counter circuit performs an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value (col. 14, lines 64-67 to col. 15, lines 1-55; Figure 11).

Referring to claim 27, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the method comprising:

- providing an AND/OR circuit connected to receive the debug data (col. 12, lines 30-62);
- providing a counter circuit connected to receive from the AND/OR circuit an increment signal that, when activated, causes the counter circuit to increment a count (col. 15, lines 56-67 to col. 16, lines 1-39); and
- providing a compare circuit for activating a match/threshold signal to the AND/OR circuit responsive to a selected block of the debug data having a designated relationship to a compare value (col. 12, lines 30-62; col. 11, lines 9-21; col. 15, lines 27-55; col. 19, lines 18-67; col. 20, lines 1-14); and

activating the increment signal by the AND/OR circuit responsive to one or more selected bits of an events signal being set (col. 15, lines 56-67 to col. 16, lines 1-2; col. 16, lines 3-39).

As to claim 28, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising activating the match/threshold signal by the compare circuit to the AND/OR circuit when the compare circuit is in match mode and the selected debug data block is equal to the compare value (col. 15, lines 27-55).

Referring to claim 29, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising activating the match/threshold signal by the compare circuit to the AND/OR circuit when the compare circuit is in threshold mode and the selected debug data block is greater than or equal to the compare value (col. 12, lines 9-29).

As to claim 30, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising:

- providing a select circuit connected to receive the debug data; and
- outputting by the select circuit to the match/threshold circuit a selected block of the debug data identified by a value of a select control signal input thereto (col. 12, lines 30-62; col. 15, lines 27-55).

Referring to claim 31, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising:

- providing a zero circuit connected to receive a portion of the selected debug data block from the

select circuit; and the zero circuit zeroing out a selected number of most significant bits ("MSBs") of the portion of the selected debug data block input thereto (col. 15, lines 56-67 to col. 16, lines 1-39).

As to claim 32, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising inputting the zeroed-out portion of the selected debug data block to the counter circuit and to the compare circuit (col. 15, lines 56-67 to col. 16, lines 1-39).

Referring to claim 33, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising the AND/OR circuit activating the increment signal when the AND/OR circuit is in AND mode and all of the one or more selected bits of the events signal are set (col. 15, lines 27-55).

As to claim 34, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising the AND/OR circuit activating the increment signal when the AND/OR circuit is in OR mode and the at least one of one or more selected bits of the events signal are set (col. 15, lines 27-55).

Referring to claim 35, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising selecting one or more bits of the events signal using a composite mask (col. 15, lines 27-55).

As to claim 36, Ranson et al. disclose a method of implementing a general purpose performance counter ("GPPC") connected to a bus carrying debug data further comprising: enabling the counter circuit; and

responsive to the counter circuit being enabled, the counter circuit performing an operation selected from a group consisting of: holding a current count value, incrementing a current count value by one, adding a specified value to the current count value, clearing the current count value, and setting the count value to a specified value (col. 14, lines 64-67 to col. 15, lines 1-55; Figure 11).

***Response to Arguments***

Applicant's arguments filed 10/9/07 have been fully considered but they are not persuasive.

Referring to claims 1, 16, and 27, Applicant argues that 'Ranson appears to teach that a hit may be indicated only when all of the selected bits in a binary field are set. To put it differently, no indication of a hit is provided in Ranson if fewer than all of the selected bits are set.' And 'There is no teaching or suggestion in Ranson of activating an increment signal when one or more selected bits are set; the only provision in Ranson is for activating an increment signal when all of the selected bits are set.'

Answer: Ranson discloses 'FIG. 13 illustrates counters 304 in detail. As can be seen in the drawing, counters block 304 includes four separate counters labeled counter 0-3. On the input side, each of counters 0-3 is coupled to increment data bus 1112, state machine output bus 1118 and HIT bus 1120. Specifically, bits 0-2 of increment data bus 1112 are coupled to counter 0, bits 3-5 are coupled to counter 1, bits 6-8 are coupled to counter 2, and bits 9-11 are coupled to counter 3. Bit 7 of state machine output bus 1118 is coupled to counter 0, bit 8 to counter 1, bit 9 to counter 2, and bit 10 to counter 3. The HIT signal is coupled to each counter.'

Each of counters 0-3 also generates an overflow bit, labeled OV 0-3 in the drawing. These four overflow bits constitute counter overflow bus 1108.' (col. 15, lines 56-67 to col. 16, lines 1-2)

Ranson also discloses 'FIG. 14 illustrates counter 0 in detail. (Counter 0 is representative of each of counters 0-3.) It is contemplated that storage elements 1406 and 1407 would be included within state machine/counters control register circuitry 346. Thus, storage element 1406 would be loaded with data by writing to state machine/counters control register circuitry 346 using the method and apparatus described above in section 2.2. Storage element 1407 may be loaded from latches 1414 and 1416 using logic such as load control logic 624, and may be read by reading from state machine/counters control register circuitry 346 using the method and apparatus described above in section 2.2 (section 2.2.2 in particular).

Counter 0 contains a thirty-two bit adder 1400, which has two addend inputs 1401 and 1403. Addend input 1401 is coupled to the output of multiplexer 1402. One input of multiplexer 1402 is coupled to a latched copy of the sum output (RSLT) of adder 1400, as shown. The other input of multiplexer 1402 is coupled to the output of storage element 1406 (initial value). Thus, depending on the state of the INIT signal, addend input 1401 will be coupled either to RSLT or to the initial value stored in storage element 1406. (Preferably, the INIT signal is generated whenever storage element 1406 is written to.) The least significant three bits of addend input 1403 are coupled to three-bit latch 1404. The twenty-nine most significant bits are coupled to ground. The input of latch 1404 is coupled to the output of multiplexer 1408. One input of multiplexer 1408 is coupled to ground, yielding an input value of "000." The other input of multiplexer 1408 is coupled to bits 0-2 of increment data bus 1112. Thus, depending on the output of AND gate 1410, the input of latch 1404 is provided either by

bits 0-2 of increment data bus 1112 or by ground. The former will be selected whenever HIT is asserted and bit 7 of state machine output bus 1118 is asserted. Thus, counter 0 may be incremented by any value between 0 and 7 depending on the content of increment data bus bits 0-2.' (col. 16, lines 3-39)

Thus, Ranson does disclose activating signal when one or more selected bits are set.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Toan Le

December 19, 2007



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